UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450

NOTICE OF ALLOWANCE AND FEE(S) DUE

22879 7590 6014/2011 HEWLETT-PACKARD COMPANY Intellectual Property Administration 3404 E. Harmony Road Mail Stop 35 FORT COLLINS, CO 80528 EXAMINER
WHITMORE, STACY

ART UNIT PAPER NUMBER

2825

DATE MAILED: 06/14/2011

 APPLICATION NO.
 FILING DATE
 FIRST NAMED INVENTOR
 ATTORNEY DOCKET NO.
 CONFIRMATION NO.

 10/6-44.625
 08/20/2003
 Christopher A. Poirier
 200/208727-1
 75/19

TITLE OF INVENTION: SYSTEM FOR AND METHOD OF CONTROLLING A VLSI ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	09/14/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1313 AND MPPE 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 1SI. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

IL PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address; and indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or bibliotic patentials of FEE ADDRESS* for maintenance fee notification

HEWLETT-PACKARD COMPANY Intellectual Property Administration

FORT COLLINS, CO 80528

3404 E. Harmony Road Mail Stop 35

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Feeds (Familing or Transmission)

I hereby certify that this Feeds (Familing is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (5/11) 273-22885, on the date indicated below.

(Depositor's name (Signate (Dat

APPLICATION NO FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO CONFIRMATION NO 10/644 625 08/20/2003 Christopher A. Poirier 200208727-1 7519 TITLE OF INVENTION: SYSTEM FOR AND METHOD OF CONTROLLING A VLSI ENVIRONMENT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE	
nonprovisional	NO	\$1510	\$300	\$0	\$1810	09/14/2011	
EXAMINER		ART UNIT	CLASS-SUBCLASS	1			
WHITMOR	RE, STACY	2825	716-136000				
Address form PTO/SI	ondence address (or Cha B/122) attached. ication (or "Fee Address 12 or more recent) attach	nge of Correspondence	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively. (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to listed, no anie will be printed.				
PLEASE NOTE: Un recordation as set fort (A) NAME OF ASSI	less an assignee is ident h in 37 CFR 3.11. Comp GNEE		THE PATENT (print or type data will appear on the pat a substitute for filing an (B) RESIDENCE: (CITY cinted on the patent):	atent. If an assignee is ic assignment.	TRY)	_	
	are submitted: No small entity discount p	permitted)		d. Form PTO-2038 is atta-	ched. required fee(s), any defic		
	s SMALL ENTITY state	is. See 37 CFR 1.27.	b. Applicant is no long	ger claiming SMALL EN			
Authorized Signature		tes Patent and Trademark	Office.	Date			

submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for rectucing this burden, should be sent to the Chief Information Officer. U.S. Patest and Trademark Officer. U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 2231-450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 2231-450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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FORT COLLINS, CO 80528

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,625	08/20/2003	Christopher A. Poirier	200208727-1	7519
22879 75	90 06/14/2011		EXAM	INER
HEWLETT-PACKARD COMPANY			WHITMOR	E, STACY
Intellectual Property Administration				
3404 E. Harmony I	Road		ART UNIT	PAPER NUMBER
Mail Stop 35			2825	

DATE MAILED: 06/14/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 2285 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 2285 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

- The information on this form will be treated confidentially to the extent allowed under the Freedom
 of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of
 records may be disclosed to the Department of Justice to determine whether disclosure of these
 records is required by the Freedom of Information Act.
- A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement neeotiations.
- 3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
- 4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
- 5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
- A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
- 7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2004 and 2006. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals
- 8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
- A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability

Application No.	Applicant(s)		
10/644,625	POIRIER ET AL.		
Examiner	Art Unit		
STACY WHITMORE	2825		

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included
herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative
of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.
1. This communication is responsive to <u>telephone conversation with Dan Hu on 6/7/2011</u> .
2. A The allowed claim(s) is/are 1, 3-8, 10-16, 18-32, renumbered per 37 CFR 1.126.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some c) None of the:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in Institution No. _____.

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the req	uirements
noted below. Failure to timely comply will result in ABANDONMENT of this application.	
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.	

4. 🔲 A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF	-
INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.	

5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

(a) I including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

 DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. Notice of References Cited (PTO-892)

2. Notice of Draftperson's Patent Drawing Review (PTO-948)

 Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date

Examiner's Comment Regarding Requirement for Deposit of Biological Material

5.	П	Notice	of	Informal	Patent	Application

Interview Summary (PTO-413),
 Paper No./Mail Date

7. X Examiner's Amendment/Comment

8.

Examiner's Statement of Reasons for Allowance

9. 🔲 Other ____

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EXAMINER'S AMENDMENT

Claims 1, 3-8, 10-16, and 18-32 are allowed over the prior art of record.

- 2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.
- Authorization for this examiner's amendment was given in a telephone interview with Dan Hu on June 7, 2011.
- The application has been amended as follows:

In the claims:

- I. Cancel claims 2, 9, and 17.
- II. Delete claims 1, 3-6, 8, 10-13, 15-16, and 18-22, 24-27, and 29, and replace with the following amended claims 1, 3-6, 8, 10-13, 15-16, and 18-22, 24-27, and 29.

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(Currently Amended) A system comprising:

an integrated circuit on a VLSI die; and

an embedded micro-controller constructed on the VLSI die, the micro-controller adapted to monitor and control the VLSI environment to optimize the integrated circuit operation;

wherein said embedded micro-controller is configured to:

monitor meniters-temperatures at a plurality of locations on the integrated circuit;

monitor one or more parameters selected from the group consisting of:
power supplied to the integrated circuit, an operating clock frequency of the integrated
circuit, a power supply voltage supplied to the integrated circuit, and a power supply
current supplied to the integrated circuit; and

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control an environment of the VLSI die based on the monitored temperatures and the one or more parameters to enhance operation of the integrated circuit.

 (Currently Amended) The system of claim 1 wherein the embedded microcontroller is configured to control eentrols at least one of the following-parameters:

temperatures at one or more locations on the integrated circuit;

the integrated circuit power supply;

the operating clock frequency of the integrated circuit;

the power supply voltage supplied to the integrated circuit; and

the power supply current supplied to the integrated circuit.

 (Currently Amended) The system of claim 1 wherein the integrated circuit comprises two or more processor cores, each core having [[a]]an integer unit and a floating point unit, the micro-controller-system further comprising:

temperature sensors at each of the integer units and floating point units on each of the cores.

- (Currently Amended) The system of claim 1 further comprising: embedded ammeters constructed on the VLSI integrated circuit-die, the ammeters comprising voltage controlled oscillators.
- (Currently Amended) The system of claim 1 further comprising: fuses that provide hardware selection of VLSI integrated circuit environment the one or more parameters that are to be monitored by the embedded micro-controller.

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8. (Currently Amended) A method for monitoring and controlling an integrated circuit comprising:

providing an embedded micro-controller on a same VLSI die as the integrated circuit; [[and]]

monitoring, and controlling a VLSI environment of the integrated circuit with the embedded micro-controller; wherein

caid embedded micro-controller menitors temperatures at a plurality of locations on the integrated circuit, and one or more parameters selected from the group consisting of: power supplied to the integrated circuit, an operating clock frequency of the integrated circuit, a power supply voltage supplied to the integrated circuit, and a power supply current supplied to the integrated circuit; and

controlling, with the embedded micro-controller, an environment of the VLSI die based on the monitored temperatures and the one or more parameters to enhance operation of the integrated circuit.

10. (Currently Amended) The method of claim 8 further comprising: controlling, by the embedded micro-controller, one or more precessor-parameters selected from the group consisting of:

temperatures at one or more locations on the integrated circuit;

the integrated circuit power supply;

the operating clock frequency of the integrated circuit; the power supply voltage <u>supplied to the integrated circuit</u>; and the power supply current supplied to the integrated circuit.

 (Currently Amended) The method of claim 8 further comprising: controlling, using the embedded micro-controller, the VLSI-environment to optimize an integrated circuit operating power level to approach a design limit. Application/Control Number: 10/644,625 Art Unit: 2825

 (Currently Amended) The method of claim 8 further comprising: monitoring, using the embedded micro-controller, a temperature in a <u>particular</u> location of the integrated circuit; and

reducing, using the embedded micro-controller, [[a]]the power supply voltage in response to an over-temperature condition in the <u>particular</u> location.

 (Currently Amended) The method of claim 8 further comprising: monitoring, using the embedded micro-controller, a temperature in a location of the integrated circuit; and

reducing, using the embedded micro-controller, a processor-the operating clock frequency in response to an over-temperature condition in the integrated circuit.

- (Currently Amended) The method of claim 8 further comprising: monitoring, using the embedded micro-controller, eurrent levels in the integrated eircuit-the power supply current using ammeters comprising one or more voltage controlled oscillators.
- 16. (Currently Amended) A computer program product comprising a <u>non-transitory</u> computer usable medium having computer readable program code embedded therein, the computer readable program code comprising:

code for controlling an embedded micro-controller constructed on a VLSI <u>die</u>
with <u>an</u> integrated circuit-die with a processor, wherein the <u>code is for controlling the</u>
micro-controller to monitors and controls a VLSI environment of the processor; where:

said embedded micro-controller monitors-monitor temperatures at a plurality of locations on the integrated circuit;

monitor one or more parameters selected from the group consisting of:
power supplied to the integrated circuit, an operating clock frequency of the integrated
circuit, a power supply voltage supplied to the integrated circuit, and a power supply
current supplied to the integrated circuit; and

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control an environment of the VLSI die based on the monitored temperatures and the one or more parameters to enhance operation of the integrated circuit.

18. (Currently Amended) The computer program product of claim 16 further comprising:

code for controlling,—by the embedded micro-controller[[,]] to control one or more integrated eircuit parameters selected from the group consisting of:

temperatures at one or more locations on the integrated circuit;

the integrated circuit power supply;

the operating clock frequency of the integrated circuit:

the power supply voltage supplied to the integrated circuit; and

the power supply current supplied to the integrated circuit.

- 19. (Currently Amended) The computer program product of claim 16 further comprising: code for controlling the VLSI-environment to optimize an integrated circuit operating power level to approach a design limit.
- 20. (Currently Amended) The computer program product of claim 16, wherein the integrated circuit comprises a processor, the method further comprising:

code for monitoring a temperature in a core of the processor; and code for reducing [[a]]the power supply voltage in response to an over-temperature condition in the core.

21. (Currently Amended) The computer program product of claim 16, wherein the integrated circuit comprises a processor, the method further comprising:

code for monitoring a temperature in a core of the processor; and

code for reducing a <u>processor-the</u> operating <u>clock</u> frequency in response to an over-temperature condition in the core.

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22. (Currently Amended) The computer program product of claim 16, wherein the integrated circuit comprises a processor, the method further comprising:

code for monitoring a temperature in a first core of the processor; and code for transferring a processing workload from the first core to a second core of the processor in response to the temperature of said first core.

24. (Currently Amended) A system for monitoring and controlling an integrated circuit comprising:

means for providing an embedded micro-controller on a same VLSI die as the integrated circuit; and

means for menitoring and-controlling a-VLSI-environment of the integrated circuit with the embedded micro-controller[[:]]to:

wherein said embedded micro-controller monitors-monitor temperatures at a plurality of locations on the integrated circuit;

monitor one or more parameters selected from the group consisting of:
power supplied to the integrated circuit, an operating clock frequency of the integrated
circuit, a power supply voltage supplied to the integrated circuit, and a power supply
current supplied to the integrated circuit; and

control an environment of the VLSI die based on the monitored temperatures and the one or more parameters to enhance operation of the integrated circuit.

- (Currently Amended) The system of claim 24 further comprising: means for controlling, using the embedded micro-controller, the VLSI environment to optimize an integrated circuit operating power level to approach a design limit.
- (Currently Amended) The system of claim 24 further comprising: means for reducing, using the embedded micro-controller, [[a]]the power supply voltage in response to an over-temperature condition at one of said plurality of locations.

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 (Currently Amended) The system of claim 24 further comprising: means for reducing, using the embedded micro-controller, a processor-the operating clock frequency in response to an over-temperature condition in the integrated circuit.

- 29. (Currently Amended) The system of claim 1 wherein said embedded micro-controller is further adapted configured to detect a difference in temperatures between said plurality of locations on the integrated circuit and redistribute workload in response to said temperature difference. --.
- 5. Newly cited prior art but not relied upon:

Gschwind US Patent 6,948,082

Rusu US Patent 6,908,227

 Any inquiry concerning this communication or earlier communications from the examiner should be directed to STACY WHITMORE whose telephone number is (571)272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stacy A Whitmore/ Primary Examiner Art Unit 2825

SAW June 8, 2011